CLAIMS

1. A semiconductor integrated circuit device comprising:

a semiconductor substrate;

a plurality of circuit elements formed in an element forming layer on said semiconductor substrate;

a plurality of terminals formed on the surface of said element forming layer and connected to predetermined said circuit elements;

a plurality of conductive layers which are respectively connected to first terminals corresponding to some terminals of said plurality of terminals and extend on said element forming layer;

protruding electrodes respectively connected to said conductive layers;

testing pads respectively connected to all or some of second terminals corresponding to the remaining terminals of said plurality of terminals; and

an insulating film which covers the surfaces of said protruding electrodes and said testing pads so as to expose said protruding electrodes and said testing pads.

2. A semiconductor integrated circuit device comprising:

a semiconductor substrate;

a plurality of circuit elements formed in an

element forming layer on said semiconductor substrate;

a plurality of terminals formed on the surface of said element forming layer and connected to predetermined said circuit elements;

a plurality of conductive layers which are respectively connected to first terminals corresponding to some of said plurality of terminals and extend on said element forming layer;

protruding electrodes respectively connected to said conductive layers;

testing pads respectively connected to all or some of second terminals corresponding to the remaining terminals of said plurality of terminals and all or some of the first terminals; and

an insulating film which covers the surfaces of said protruding electrodes and said testing pads so as to expose said protruding electrodes and said testing pads.

3. The semiconductor integrated circuit device according to claim 1 or 2, wherein said conductive layers are metal wirings, said insulating film is formed on said each metal wiring, and an insulating film is further formed below said each metal wiring.

4. The semiconductor integrated circuit device according to claim 3, wherein said insulating film and said further insulating film are respectively formed of

different materials, and said insulating film is formed of a material higher in elastic modulus than said further insulating film.

5 The semiconductor integrated circuit device according to claim 3, wherein said insulating film is a film which contains an organic substance.

6. The semiconductor integrated circuit device according to claim 5, wherein the film containing the organic substance is a polyimide film, a fluorocarbon resin film, or an elastomer film which contains a silicon or acrylic rubber material.

7. The semiconductor integrated circuit device according to 1 or 2, wherein said testing pads are placed just above said terminals corresponding thereto.

8. The semiconductor integrated circuit device according to claim 7, wherein said testing pads are regularly placed in the central portion of said semiconductor substrate, and said protruding electrodes are regularly placed outside said testing pads respectively.

9. The semiconductor integrated circuit device according to claim 1 or 2, wherein said testing pads

extend on said insulating film.

10. A method of manufacturing a semiconductor integrated circuit device, comprising:

a first step for constituting a required circuit in an element forming layer on a semiconductor wafer, forming a plurality of terminals connected to said predetermined circuit elements on the surface of the element forming layer, and causing a plurality of conductive layers to be respectively connected to first terminals corresponding to some of the plurality of terminals and to extend over the element forming layer;

a second step for forming protruding electrodes connected to said conductive layers;

a third step for connecting testing pads to all or some of second terminals corresponding to the remaining terminals of the plurality of terminals respectively to form the testing pads;

a fourth step for inspecting the required circuit formed in the element forming layer;

a fifth step for performing burn-in; and

a sixth step for dicing the wafer.

11. A method of manufacturing a semiconductor integrated circuit device, comprising:

a first step for constituting a required circuit in an element forming layer on a semiconductor wafer,

forming a plurality of terminals connected to said predetermined circuit elements on the surface of the element forming layer, and causing a plurality of conductive layers to be respectively connected to first terminals corresponding to some of the plurality of terminals and to extend over the element forming layer;

a second step for forming protruding electrodes connected to said conductive layers;

a third step for connecting testing pads to all or some of second terminals corresponding to the remaining terminals of the plurality of terminals and all or some of the first terminals respectively to form the testing pads;

a fourth step for inspecting the required circuit formed in the element forming layer;

a fifth step for performing burn-in; and

a sixth step for dicing the wafer.

Sub A4

12. The method according to claim 10 or 11, further including a seventh step for substituting a defective portion with a relieving circuit according to the result of inspection by said fourth step.

13. The method according to claim 10 or 11, wherein after the protruding electrodes are formed in said second step and the testing pads are formed in said third step, the burn-in in said fifth step is effected on pieces

diced in said sixth step.

Sub A4

14. The method according to claim 10 or 11, wherein after the testing pads are formed in said third step, the bur-in is executed in said fifth step, the protruding electrodes are formed in said second step and the dicing is performed in said sixth step.

15. A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface on which an integrated circuit and a plurality of first electrodes are formed, said plurality of first electrodes being arranged at fist intervals;

a first insulating film which covers the main surface of said semiconductor chip;

a plurality of first wiring layers formed on said first insulating film and having one ends respectively connected to said plurality of first electrodes and the other ends respectively arranged at second intervals larger than said first intervals;

a plurality of first conductor layers respectively electrically connected to said plurality of first wiring layers and formed on the other ends of said plurality of first wiring layers;

B

a plurality of second conductor layers respectively electrically connected to said plurality of first wiring

layers and formed on said plurality of first wiring layers, said plurality of second conductor layers being respectively placed in positions different from the other ends; and

a plurality of protruding electrodes respectively formed on said plurality of first wiring layers,

wherein said plurality of first conductor layers and said plurality of second conductor layers are respectively formed of a conductor film formed in the same steps.

16. The semiconductor integrated circuit device according to claim 15, wherein said plurality of first conductor layers are under conductor layers for said plurality of protruding electrodes, and said plurality of second conductor layers are testing conductor layers for performing an electrical test.

17. The semiconductor integrated circuit device according to claim 15, wherein one ends of said plurality of first wiring layers are respectively connected to said plurality of first electrodes through a plurality of openings defined in the first insulating layer.

18. The semiconductor integrated circuit device according to claim 17, further including a second insulating film, which is formed below said first

insulating film and covers the main surface of said semiconductor chip, and wherein said second insulating film has a plurality of openings which expose said plurality of first electrodes.

19. The semiconductor integrated circuit device according to claim 18, wherein said first insulating film is an organic insulating film and said second insulating film is an inorganic insulating film.

20. The semiconductor integrated circuit device according to claim 19, wherein said first insulating film contains a polyimide film, and said second insulating film contains a nitride silicon film.

21. A semiconductor integrated circuit device comprising:

a semiconductor substrate;

a circuit element formed on said semiconductor substrate;

a first conductive layer formed on said semiconductor substrate and connected to said circuit element;

a second conductive layer which is formed on said semiconductor substrate and constitutes testing pads;

bumps formed on sad first conductive layer and each connected to said first conductive layer; and

an organic film formed between said semiconductor substrate and said first conductive layer and between said semiconductor substrate and said second conductive layer,

wherein said first conductive layer and said second conductive layer are connected to each other.

22. A semiconductor integrated circuit device comprising:

a semiconductor substrate;

a circuit element formed on said semiconductor substrate;

a conductive layer, which is formed over said semiconductor substrate and has a wiring portion and a testing pad portion and which is connected to said circuit element;

bumps formed over said wiring portion and connected to said wiring portion; and

an organic film formed between said semiconductor substrate and said testing pad portion.

23. A semiconductor integrated circuit device comprising:

a semiconductor substrate;

a first circuit element and a second circuit element formed on said semiconductor substrate;

wirings formed over said semiconductor substrate

and each connected to said first circuit element;

bumps formed over said wirings and connected thereto; and

a conductive layer, which is formed over said semiconductor substrate and connected to said second circuit element and which constitutes testing pads,

wherein said conductive layer is electrically isolated from any bump.

24. A semiconductor integrated circuit device comprising:

a semiconductor substrate;

a semiconductor integrated circuit element formed in said semiconductor substrate;

a wiring formed on said semiconductor substrate and connected to said semiconductor integrated circuit element;

a bump formed on said wiring and connected thereto; and

a conductive layer, which is formed on said semiconductor substrate and connected to said semiconductor integrated circuit element and which constitutes each of testing pads,

wherein when said semiconductor integrated circuit element is tested, said testing pad is electrically connected to the outside of said semiconductor integrated circuit device, and

when said semiconductor integrated circuit element is in normal operation, said testing pad is electrically disconnected from the outside of said semiconductor integrated circuit device.

SUB A5

25. A semiconductor integrated circuit device comprising:

a semiconductor substrate;

integrated circuit elements formed on said semiconductor substrate;

a plurality of wirings formed on said semiconductor substrate and connected to said integrated circuit elements;

a plurality of bumps formed on said plurality of wirings and provided in association with said plurality of wirings;

a conductive layer, which is formed on said semiconductor substrate and connected to said integrated circuit elements and which is formed as each of testing pads; and

an organic film placed on said semiconductor substrate and formed below said plurality of wirings,

wherein when said each integrated circuit element is tested, said each testing pad is electrically connected to the outside of said semiconductor integrated circuit device, and

when said each integrated circuit element is in

normal operation, said each testing pad is electrically disconnected from the outside of said semiconductor integrated circuit device.

Sub B7

26. A semiconductor integrated circuit device comprising:

a semiconductor substrate;

a first circuit element and a second circuit element formed on said semiconductor substrate;

a wiring formed on said semiconductor substrate and connected to said first circuit element;

a bump formed on said wiring and connected thereto;

a first conductive material, which is formed on said semiconductor substrate and connected to said first circuit element and which constitutes a first testing pad; and

a second conductive material, which is formed on said semiconductor substrate and connected to said second circuit element and which constitutes a second testing pad,

wherein when said first circuit element and said second circuit element are tested, said first testing pad and said second testing pad are electrically connected to the outside of said semiconductor integrated circuit device, and

when said first circuit element and said second circuit element are in normal operation, said first

testing pad is electrically connected to the outside of said semiconductor integrated circuit device through said bump, and said second testing pad is electrically disconnected from the outside of said semiconductor integrated circuit device.

SUB B5

27. A semiconductor integrated circuit device comprising:

a semiconductor substrate;

an integrated circuit formed on said semiconductor substrate;

a wiring formed on said semiconductor substrate and connected to said integrated circuit;

a bump formed on said wiring and connected thereto;

a first conductive layer, which is formed on said semiconductor substrate and connected to said integrated circuit and which constitutes a first testing pad; and

a second conductive layer, which is formed on said semiconductor substrate and connected to said integrated circuit and which constitutes a second testing pad,

wherein said first conductive layer and said wiring are connected to each other, and

when said integrated circuit is tested, said first testing pad and said second testing pad are electrically connected to the outside of said semiconductor integrated circuit device and

when said integrated circuit is in normal operation,

said first testing pad is electrically connected to the outside of said semiconductor integrated circuit device and said second testing pad is electrically isolated from the outside of said semiconductor integrated circuit device.

SUB B5

28. A semiconductor integrated circuit device comprising:

a semiconductor substrate;

integrated circuit elements formed on said semiconductor substrate;

a plurality of wirings formed over said semiconductor substrate and connected to said integrated circuit elements;

a plurality of bumps formed over said plurality of wirings and provided in association with said plurality of wirings;

a conductive layer, which is formed over said semiconductor substrate and connected to said each integrated circuit element and which constitutes each of test pads; and

a film containing an organic material formed between said semiconductor substrate and said plurality of wirings and between said semiconductor substrate and said conductive layer,

wherein when said integrated circuit element is tested, said test pad is electrically connected to the

Sub B7

outside of said semiconductor integrated circuit device, and

when said integrated circuit element is in normal operation, said test pad is electrically disconnected from the outside of said semiconductor integrated circuit device.